(12) UK Patent Application (19) GB (11) 2 029 145 A

(21) Application No 7922592
(22) Date of filing
28 Jun 1979
(23) Claims filed
28 Jun 1979
(30) Priority data
(31) 2828836
(32) 30 Jun 1978
(33) Fed Rep of Germany (DE)
(43) Application published
12 Mar 1980
(51) INT CL³ G11C 17/00
(52) Domestic classification
H3T 2B7 2T3F 3T3S MX
(56) Documents cited
None
(58) Field of search
H3T

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(54) Non-volatile word-wise electrically erasable stores

(57) A word-wise erasing non-volatile store has a matrix of storage cells (100, 200, 300, 400) e.g. field effect transistors with floating gates. Appropriate voltages for erasure are applied to the gates of the selected cells (via transistors 166, 366) and to their sources (via transistors 122, 222).

In order to obviate the need for an external timer and to avoid the erasing voltages being applied for longer than necessary, analysis means (129, 229) are provided for each cell, to indicate when the cell has reached its erased state. As shown these each comprise a flip-flop which senses the resulting drop in drain voltage, and changes state to terminate (via gate 125 and transistor 121, or 225 and 221) application of erasing pulses to the source of the cell.

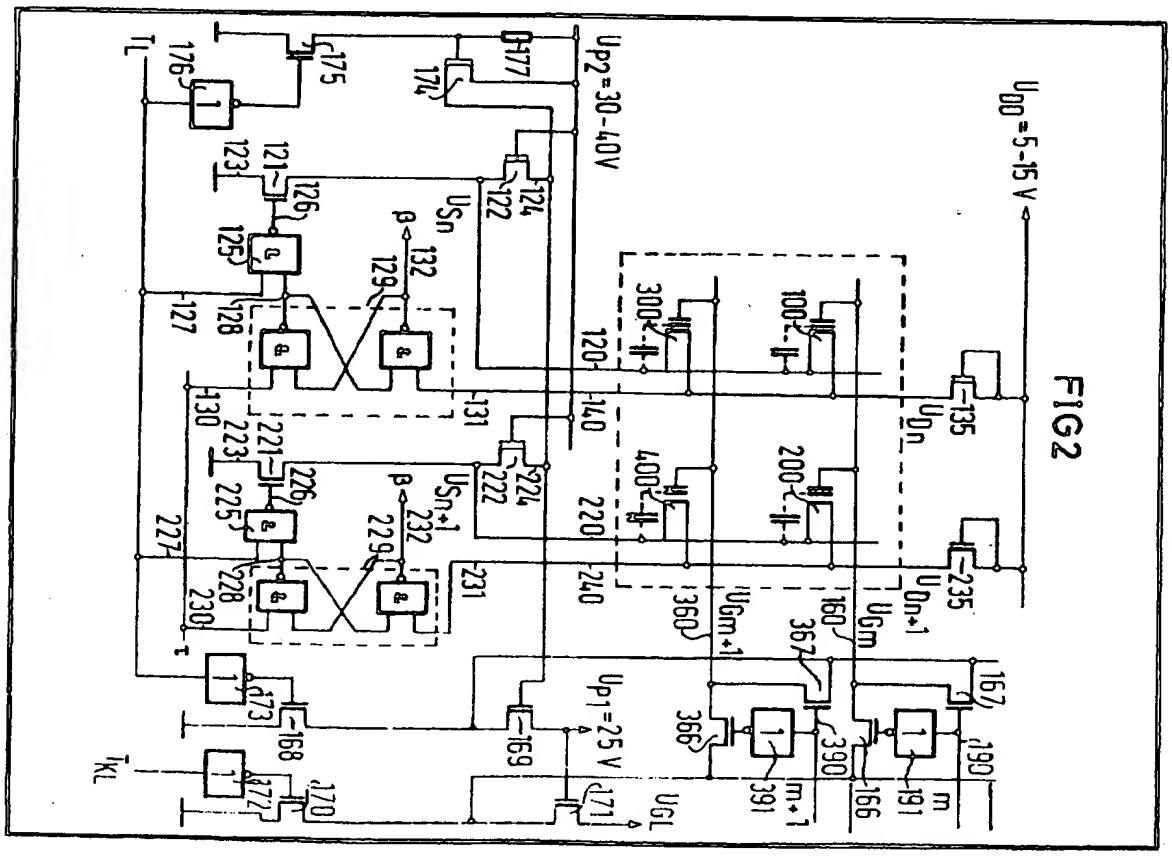

FIG2

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FIG1

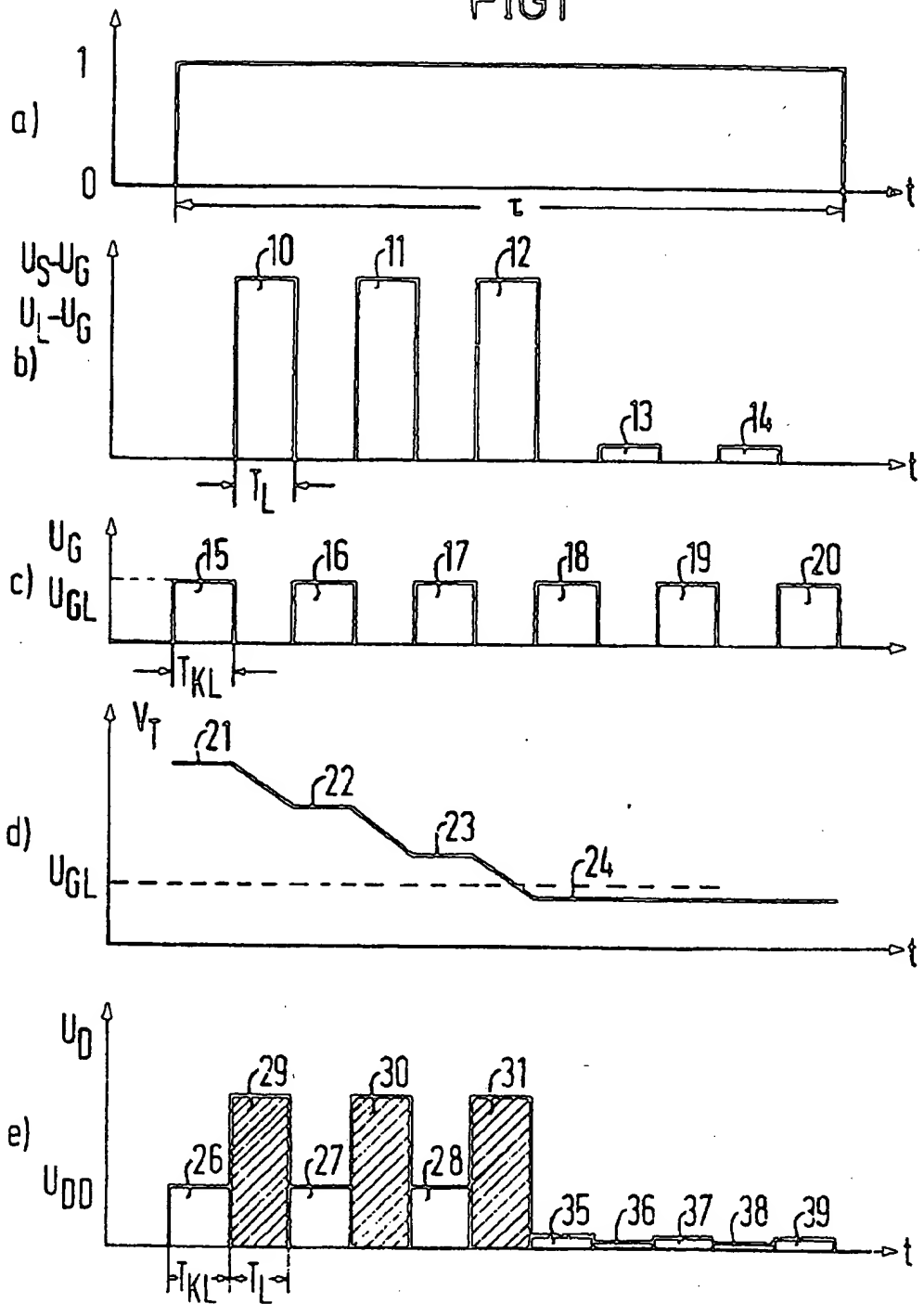

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FIG2

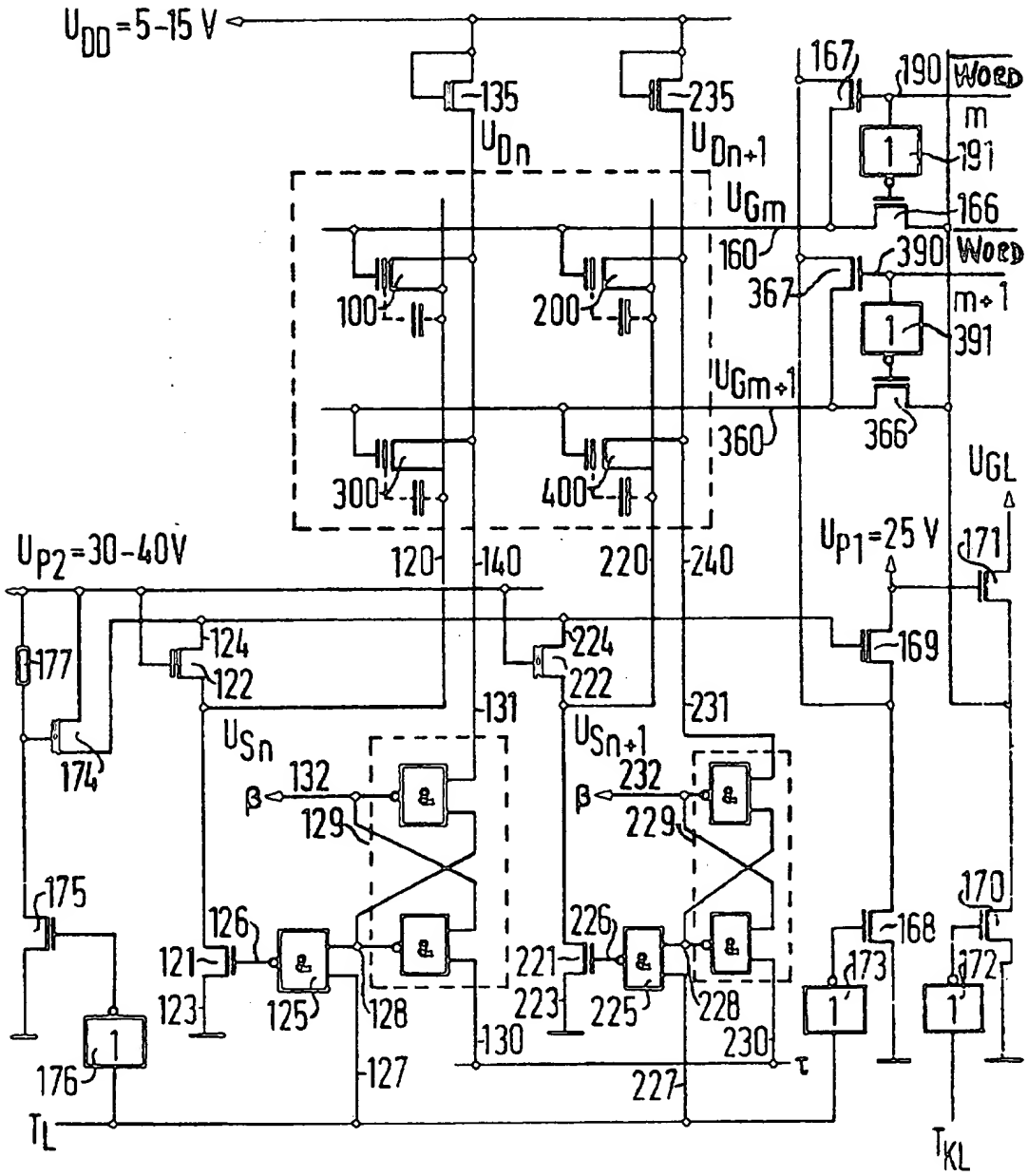

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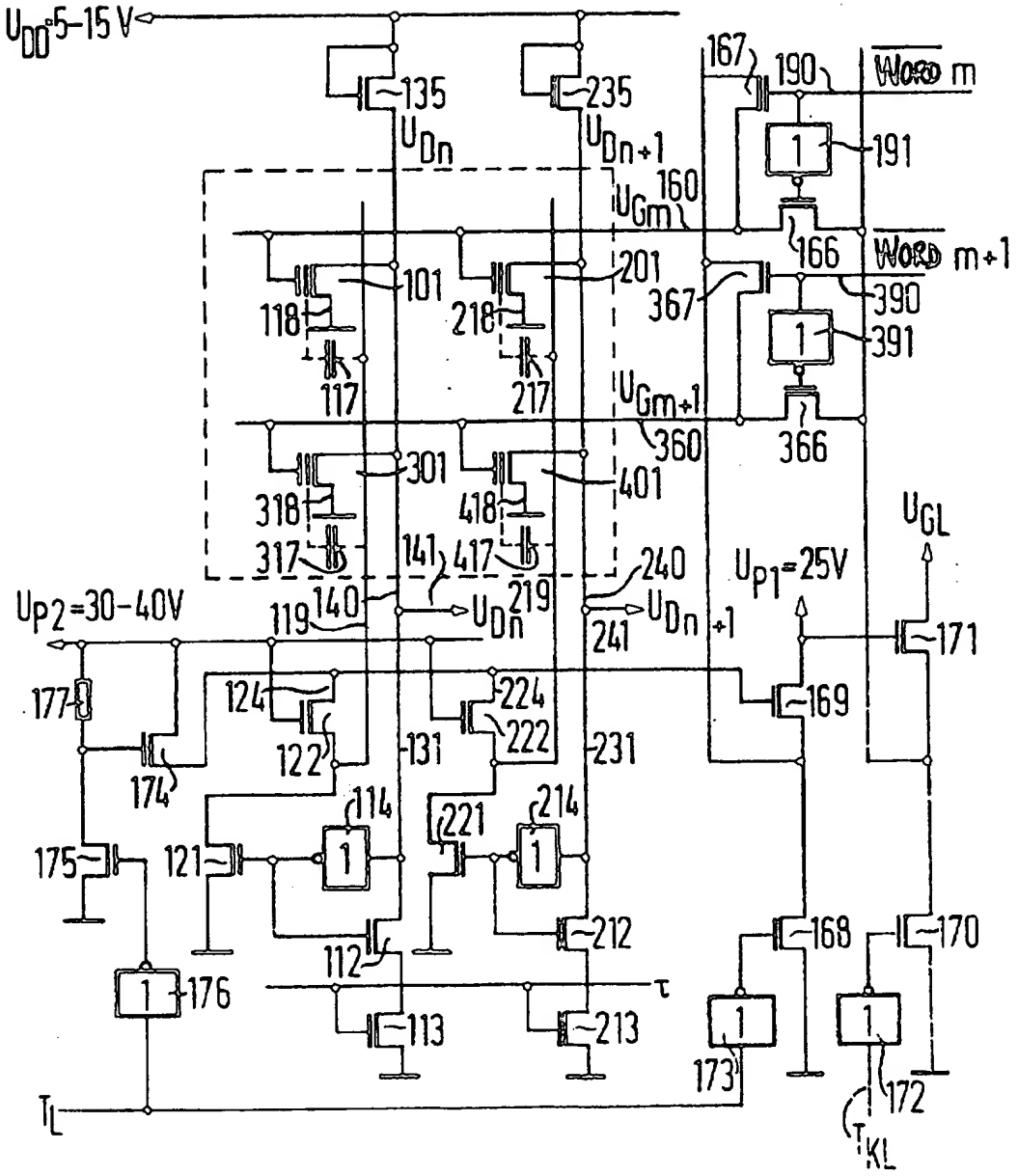
FIG3



SPECIFICATION

Non-volatile word-wise electrically erasable store

The invention relates to a non-volatile store comprising storage cells arranged in the form of a matrix and which can be electrically erased word-wise.

IEEE Transactions on Electron Devices Vol. ED-24, No. 5, May 1977, pages 606 to 610 discloses a floating-gate storage cell for the construction of non-volatile, electrically reprogrammable stores. In these field effect transistors a floating storage gate which is completely insulated and a controllable control gate are arranged above the channel path; the control gate covers the entire channel path although the floating gate covers only a part thereof. This so-called split-gate structure avoids errors during the read-out of erased storage cells having depletion characteristics. The floating storage gate is charged by means of channel injection. For this purpose electrons are accelerated in a short channel and conveyed to the storage gate by means of an additional, transverse electrical field. The storage gate is discharged or erased by back-tunnelling of the electrons with a high voltage connected between the control gate and a diffusion zone.

German patent application P 27 43 422.6 and the corresponding United Kingdom patent application No. 38106/78 (serial No. 2 005 915A) describe a non-volatile store designed in floating-gate technology and which can be erased word-wise. Both the charging and discharging of the floating gate is carried out by means of a direct transfer of electrons between the floating gate and the substrate, when a high electric field of suitable polarity is connected between the floating gate and a diffusion zone.

In all previously known stores which are constructed from the described storage cells, the erasure time is determined and set up via an external timer. The erasure times must be selected taking into account production-dependent fluctuations in the erasing properties of the individual cells not only within one chip, but also in respect of various production batches. It is also necessary to take into account the tolerance fluctuations resulting from the timer itself. Therefore it cannot normally be avoided that at least some of the storage transistors are erased into the depletion state. These over-erased storage cells represent an undesired shunt to the selected storage transistors during read-out. Therefore as a rule the storage cells of an electrically erasable store must be provided with an additional selector transistor. Although in many cases this selector transistor can be combined with the storage transistor to form a split-gate structure, this in turn increases the technological problems and reduces the production yield. Furthermore the high erasure times of the described stores involve the danger of disturbance to neighbouring words and frequently also impair the programming properties, in particular in the case of storage cells in which the recording process is carried out by means of channel injection. High erasure times also reduce the number of permissible programme erase cycles and thus the life of a store of this type.

According to the present invention there is provided a non-volatile semiconductor store which can be electrically erased word-wise, comprising a matrix of storage cells, control means operable to apply voltages to selected storage cells for erasure thereof, and monitoring means arranged, in use, to monitor, the state of the storage cells during erasure and to recognise when each cell being monitored reaches its erased state.

By this means, the risk of the transistors of the storage cells which are to be erased reaching the depletion state is reduced. Thus such stores can be constructed from one-transistor storage cells which in turn results in the advantage of a smaller space requirement of corresponding storage chips. Reduction of erasure time for storage cells also results in the advantage of a reduced oxide change during the erasure process which itself can result in an increased number of record-erase cycles, i.e. an increased life of the store.

The store corresponding to the invention also has the advantage that, with a minimal circuitry outlay, it permits the overall erasure time to be fixed, as described in our co-pending United Kingdom patent application No. 7922590 Serial No. 2028615 (VPA 78 P 1110). This avoids the need for an external timer.

Preferably the control means is arranged in operation to supply erasing voltages to the selected storage cells intermittently in the form of pulses, and the monitoring means is arranged to monitor the state of the storage cells during the intervals between the pulses.

This measure has the advantage of allowing one-transistor cells to be used to construct a store. Furthermore the splitting of the overall erasing pulse into a number of individual pulses results in the advantage of a lesser overall crystal heating during the erasure process and thus a reduction in damage which can occur from this heating during the erasure process. The significance of this advantage will increase in proportion to the erasing current, i.e. the greater the heating is during the overall erasure process. Erasing currents of this kind are produced for example by undesired breakthrough effects.

In the case of cells which do not possess an erasing zone which is electrically insulated from the channel zone, simultaneous erasure and check read-out cannot be effected inas-

much as for example in the case of n-channel storage cells erasure requires the connection of a high positive voltage to the source, whereas check read-out requires that the source be connected to earth. In *p*-channel technology similar applies with exchanged signs of the voltages. These two conditions cannot be fulfilled simultaneously. However, the splitting of the erasing voltages into a time sequence of individual pulses allows check read-out to be carried out during the intervals between the erasing pulses. Alternatively, it may be arranged that the control means is arranged in operation to supply erasing voltages to the selected storage cells continuously whereby erasure and monitoring take place simultaneously.

Preferably the monitoring means is arranged, in operation to recognise erasure as being complete when, during a check read-out process, the storage cell carries a threshold voltage V_T ("0") where $|V_T("0")|$ is smaller than or equal to $|U_{GL}|$, where U_{GL} is a given threshold value of the storage cell which is bening used.

In the case of storage cells constructed in *n*-channel technology, the aforementioned relationship between the lower threshold voltage value $V_T("0")$ and the check read-out voltage $U_{GL} > V_T("0") > 0$ permits termination of the erasure process before the cell which is to be erased is able to reach the depletion state. In order to achieve this, the duration of the individual erasing pulses should be such that the cell which is to be erased is unable to reach the depletion state during an erasing pulse but is previously disconnected.

Continuous erasure and simultaneous read-out can be effected in storage cells of the floating-gate type which possess an erasing window which is electrically insulated from the channel zone, so that in *n*-channel technology the source voltage can amount to 0 V for the entire erasing time whereas the insulated diffusion zone in the erasing window carries a high positive voltage. A cell of this kind is described in German Offenlegungsschrift 26 43 987 and the corresonding United Kingdom patent application No. 38106/78 (serial No. 2 005 915A).

Recording with bit-wise individual recording time is of comparatively less significance in practice. During programming all the threshold voltages asymptotically approach *n* values, the fluctuations in which are on the one hand small and whose exact value is on the other hand unimportant. Excessive recording, similarly to over-erasure, into the depletion state does not exist. For recording the drive circuit may expediently be designed in the manner described in our co-pending United Kingdom patent application No. 79 22590 Serial No. 2028615 (VPA 78 P 1110), in order to avoid the need for an external timer and at the same time to achieve a determinate minimum value of the state "1".

Conveniently, completion of erasure may be monitored in that within a check read-out process, with a gate voltage U_{GL}, the erased state is indiciated by a drop in the absolute value of the drain voltage $|U_D|$.

As is known the conductivity of floating-gate transistors changes in accordance with the charge state of the floating gate. This change in the state of conductivity can be used as a signal that the erasing state has ended. When drain lines are connected bit-wise and are connected to a specific read-out voltage, during the erasing time, in the check read-out process the drains float up to a specific voltage value when the transistors have been sufficiently erased. This is subject to the condition that the non-selected storage cells which are not allowed to reach the depletion state, should be fed with a sufficiently low gate voltage of approximately 0 V. Conveniently, it may be arranged that those drain output signals which indicate the end of the erasing time of a storage cell are used to disconnect the erasing voltage connected to this cell.

In a preferred arrangement the gate lines of the field effect transistors used to construct the storage cells lead from word to word whereas the drain lines lead from bit to bit. When a cell is used which possesses an electrically insulated diffusion zone within the erasing window, such as described for example in the German Offenlegungsschrift 26 43 987/United Kingdom patent application No. 40244/77 (serial No. 1550784), the erasing window lines always run from bit to bit, and in this case the source lines are connected to zero potential. On the other hand, in the cells which do not possess insulated erasing zones the source lines are separated from one another bit-wise.

The gate voltage which is required as a given threshold voltage value (U_{GL}) for check read-out during erasure, and the gate voltage for the read-out of the store (U_{GR}) may, if desired, be obtained from one and the same potential divider so that U_{GL} is always smaller than U_{GR}.

This measure ensures a safe minimum clearance between the gate voltage U_{GR} during read-out and the threshold voltage $V_T("0")$ of the erased state of a storage cell, where $V_T("0")$ is smaller than U_{GR}. Thus read-out reliability can be improved. Tolerance-dependent differing erasing properties of a storage cell within a store do not influence the reliability of read-out, but merely the length of the erasing process. Since this measure determines the unprogrammed state relative to the read-out voltage, the width of the electric erasing window, i.e. the potential difference between the gate voltage during check read-out in erasure U_{GL} and the state "1" of the programmed state can be reduced. Advanta-

geously this allows the voltages during programming to be low or the programming time to be particularly short. This measure also allows the electric window to be arranged in a given threshold value range.

Some exemplary embodiments of the invention will now be described with reference to the accompanying drawings. The embodiments shown in the drawings are of stores constructed in *n*-channel technology, which can also be converted to *p*-channel technology by changing the signs accordingly. In the drawings:—

Figures 1a-e illustrate voltages applied a storage transistor which is erased by means of pulses during the erasing time τ of a storage row;

Figure 2 illustrates a drive circuit for a store corresponding to the invention composed of one-transistor cells with source-side recharging zone during erasure; and

Figure 3 illustrates a drive circuit of a store corresponding to the invention composed of one-transistor cells with an insulated recharging zone during erasure.

Fig. 1*a* shows the erasing time τ of the storage row during which the flip-flop inputs 130, 230 from Fig. 2 and the gates of the transistors 113, 213 from Fig. 3 are raised from the voltage state "0" into the voltage state "1".

Fig. 1*b* illustrates the time-based curve of the difference between the source potential U_S and gate potential U_G and between the recharging potential U_L and gate potential U_G of a transistor cell such as is provided in a store corresponding to Fig. 2 and Fig. 3. In this case high voltage pulses are emitted in sufficient numbers to a cell which is to be erased, here indicated by the pulses 10, 11, 12, until the cell which is to be erased reaches a specific threshold voltage value V_t("0" < U_{GL}. Then, in order to terminate the erasing time τ of the overall storage row, only very small voltage pulses, indicated by 13, 14, or no further voltage pulses are emitted to the cell which is to be erased.

Fig. 1*c* illustrates the time-based curve of the gate voltage U_G during the intervals between the erasing pulses. The entire erasing pulse interval is filled by the check read-out time T_{KL}. The check read-out time can also be shorter than the erasing pulse interval, and is merely required to lie within an erasing pulse interval. In the following drawings and exemplary embodiments the check read-out time T_{KL} has been selected to be of equal length to the erasing pulse interval. The check read-out pulses 15 to 20 possess a fixed voltage value U_{GL} which determines a specific, predetermined threshold voltage value of the cell being used and is substantially smaller than the level of the erasing pulses illustrated in Fig. 1*b*.

Fig. 1*d* illustrates the threshold voltage V_T of a storage cell in dependence upon the time t. Here, during the erasing pulses 10, 11, 12 from Fig. 1*b* the threshold voltage falls from the initial level 21 in turn to the levels 22, 23, 24. The level 24 is lower than the given gate voltage U_{GL} which is entered as a broken line in Fig. 1d. As can be seen from Figs. 1*b* and 1*d*, when a level 24 which lies below a voltage U_{GL} has been reached, no further erasing pulses are emitted to a cell which is to be erased so that no further change occurs in the threshold value voltage V_T from this time onwards.

Fig. 1*e* illustrates the drain voltage U_D in dependence upon the time t within the erasing time τ of a storage row (see Fig. 1*a*). During the check read-out time T_{KL}, the drain voltage U_D is equal to the relatively small read-out voltage U_{DD} connected to the drain. During the erasing pulse time T_L, in accordance with the drive process within the shaded zones 29, 30, 31 the drain voltage can be high or low. During the erasing pulse time T_L the level of the drain voltage has no influence upon the junction of the described circuit. Following a drop in the threshold voltage V_T (see Fig. 1*d*) below the value U_{GL}, the storage cells which are to be erased become conductive. Thus during the check read-out time T_{KL} the drain voltage U_D falls to the values 35, 36, 37, 38, 39 which are approximately equal to 0.

Fig. 2 illustrates a store having one-transistor storage cells of the type not having an insulated diffusion zone in the region of the erasing window, along with the associated drive circuitry. For reasons of clarity, only four storage cells 100, 200, 300, 400, and associated drive circuits have been illustrated. The *n*-th bit wise connected source line 120 is connected to the sources of the storage cells 100 and 300. Correspondingly the *n*+ 1-th source line 220 is connected to the sources of the cells 400 and 200. The *n*-th bit-wise connected drain line 410 carries a potential U_{Dn} and is connected to the drains of the storage cells 100 and 300, whereas the bit-wise connected drain line 240 carries a potential U_{Dn+1} and is connected to the drains of the storage cells 200 and 400. The gate line 160 which carries a gate voltage U_{Gm} is connected to the gates of the storage cells 100 and 200, whereas the gate line 360 which carries a gate voltage of U_{Gm+1} is connected to the gates of the storage cells 300 and 400.

The source line 120, 220 is switchable by means of transistors 122, 222 and 121, 221 between a low voltage (of approximately 0 V) connected to the terminal 123, 223 and a high voltage (of approximately 25 to 40 V) connected to the terminal 124, 224 respectively. The source line 120, 220 carries the lower potential when the transistor 121, 221 is conductive. The gates of each transistor

121, 221 is controlled by the output 126, 226 of a NAND gate 125, 225. One input 127 of the NAND gate 125 and one input 227 of the NAND gate 225 always carries a "1" during the erasing pulse time T_L, which has been symbolically represented in the drawing by T_L, whereas at all other times this terminal carries a "0". The second input 128, 228 of the NAND gate 125, 225 is connected to an output of a flip-flop 129, 229. One input 130, 230 of the flip-flop 129, 229 is supplied with a signal which is a "1" for the entire erasing time τ, and "0" at all other times. The second input 131, 231 of the flip-flop 129, 229 is connected to the corresponding drain line 140, 240. One output 132, 232 of the flip-flop 129, 229 is connected to a common AND gate β (not shown in the drawings), whose output serves to terminate the signal τ (applied to the inputs 130, 230 for the period of the erasing phase) when the erasing process is completed in all the cells within a storage row. For the entire erasing time τ the input 130, 230 of the flip-flop 129, 229 is constantly supplied with "1". Accordingly the second input 131, 231 of the flip-flop 129, 229 is likewise supplied with a positive voltage U_{DD} of approximately 5 to 15 V via the load transistor 135, 235 for the entire erasure phase. Thus the flip-flop output 128, 228 carries a "1" until the selected cell of the associated bit has been erased. For the duration of the erasing pulses T_L the second input 127, 227 of the NAND gate 125, 225 carries a "1" whereas at all other times it carries a "0". In this way the output 126, 226 of the NAND gate 125, 225 carries a "0" during the erasing pulses, i.e. the transistor 121, 221 is turned off, and thus, assuming that $U_{p2} = 30$ V to 40 V, the source line 120, 220 is connected via the transistors 122, 174 and 222, 174 to a high positive potential (25 V – 40 V). On the other hand, during the intervals between the erasing pulses the input 127, 227 carries a "0" and thus the outputs 126, 226 of the NAND gate 125, 225 carry a "1". In this way the transistor 121, 221 is rendered conductive and during the intervals between the erasing pulses low voltages of approximately 0 V are applied via the transistor 121, 221 to the source line 120, 220 so that check readout can be effected with a low voltage connected to the source and a small positive voltage (U_{DD}) connected to the drain. When a selected cell in a bit, e.g. in the n-th bit, has been sufficiently erased, this cell becomes conductive. As a result, in the following interval the drain voltage U_{Dn} falls to a small voltage of approximately 0. From this time onwards the input 131 of the flip-flop 129 carries a "0", whereas for the entire erasing time τ of the store the second flip-flop terminal 130 carries a "1". The flip-flop output 132 thus switches to "1" whereas the second flip-flop output applies a "0" to the input 128 of the NAND gate 125. The "1" present at the output 132 can be applied to an input of an AND gate β (not shown), whose output signal, at the end of the erasing time of the last selected cell, emits a signal which can be used to disconnect the signal for the erasing time τ. For the whole of the remainder of the erasing time the output 226 which is connected to the NAND gate 125 always carries a "1", so that the transistor 121 is conductive and thus the source line 120 carries a potential of approximately 0 V for the whole of the remainder of the erasing phase of the store. The erasing time of each individual cell of the row being erased is thus individually disconnected and at the end of the erasing time of the last cell and AND gate β—via its output signal—disconnects the electric signal for the erasing time τ of the selected storage row. Not until the end of the overall erasing process are the flip-flops reset; this occurs as soon as, during the erasing time, simultaneously to the zero levels at the inputs 130, 230, the drain voltages U_{Dn}, U_{Dn+1} connected to the inputs 129, 229 at least temporarily become "1".

In the gate drive circuit $m+1$ will be assumed to be a selected storage row, whereas m will be assumed to be a non-selected word. The word selection is carried out with a logic "0" from an address decoder, indicated by the signal $\overline{\text{Word}}$.

Thus the input 390 is supplied with a "0" so that the transistor 366 is switched on via the inverter 391 whereas the transistor 367 is simultaneously disabled. Thus during the erasing pulse time T_L (synonymous with check read-out time T_{KL} "0") the gate line 360 carries a gate voltage U_{Gm+1} of approximately 0 V via the transistor 366 across the transistor 170 which has been switched through by means of T_{KL} and the inverter 172. Thus during the erasing pulse time T_L a voltage of approximately 0V is connected to the gate line of a selected word, whereas a high positive voltage of 25 V to 40 V is simultaneously connected to the source lines, as has already been shown. On the other hand, during the erasing pulse time the gates of non-selected neighbouring words e.g. of $\overline{\text{Word}}$. m carry a high positive voltage so that no disturbances to neighbouring words occur during erasure. The input 190 of the non-selected word in fact carries a "1" so that the transistor 166 is turned off via the inverter 191 whereas the transistor 167 is rendered conductive and the transistor 168 switched off via the inverter 173 during the erasing pulse time T_L. Thus the gate line 160 of a non-selected word is connected via the transistor 169 to a high positive voltage of approximately $U_{P1} = 25$ V. Consequently the gate voltages of the neighbouring words carry such a high positive potential that the voltage differences U_S –

U_G = 0 V to 15 V are not adequate to erase the neighbouring cells. The reason why the transistor 169 is rendered conductive during the erasing pulse time T_L is that during this time the transistor 175 is held off by the inverter 176 and the transistor 174 is turned on through via the resistor 177 and thus conducts a positive voltage of approximately U_{P2} = 30 V to 40 V to the gate of the transistor 169.

During the check-read-out time T_{KL} which takes place in the intervals between the the erasing pulses, the transistor 170 is non-conductive on account of the inverter 172. The gate line 360 of the selected word, Word. $m+1$, is thus connected via the transistor 171 to the check read-out voltage U_{GL} which can be obtained from a potential divider (as described for example in our co-pending United Kingdom patent application No. (VPA)).

During the check read-out time T_{KL} the gate line 160 of a non-selected word is connected to a voltage U_{Gm} of approximately 0 V via the transistors 167 and 168 and due to the fact that the transistor 169 is off. This eliminates disturbances in neighbouring words during the check read-out process.

The transistor 169 is off because during T_{KL} the input of the inverter 176 carries a "0" and its output carries a "1" so that the transistor 175 is conductive and the transistor 174 (resistance of 177> resistance of switched through transistor 175) is off, which results in the fact that the transistor 169 is also off.

Fig. 3 illustrates a drive circuit for a floating-gate one-transistor cell with an insulated recharging zone in the region of the erasing window. For reasons of clarity only four storage cells 101, 201, 301, 401 and associated drive circuit have been shown. The storage cells 101, 201, 301, 401 which have been used are of the type described in German Offenlugungsschrift 26 43 987.

As can be seen from Fig. 3, various parts of the drive circuit are identical to parts of the drive circuit corresponding to Fig. 2. Identical circuit elements have been provided with like references as in Fig. 2.

The gate drive circuit in Fig. 3 is identical to that in Fig. 2, and consequently reference should be made to the description relating to Fig. 2.

Fig. 3 differs from Fig. 2 in that in Fig. 3 the storage cells 101, 201, 301, 401 each possess a recharging zone which is electrically insulated from the source, indicated by 117, 217, 317, 417, which, similarly to Fig. 2, can be switched over bit-wise by means of the recharging line 119, 219 by means of the transistors 121, 122 and 221, 222 between a low voltage of approximately 0 V and a high voltage of approximately 25 V to 40 V. The sources 118, 218, 318, 418 which are electrically insulated from this recharging zone are each earthed, on the other hand. Similarly to the drains of the drains of the storage cells illustrated in Fig. 2, the drains of the storage cells in Fig. 3 are connected by means of a drain line 140, 240 leading from bit to bit. The function of the flip-flop 129, 229 and the NAND gate 125, 225 connected thereto as illustrated in Fig. 2 is assumed in Fig. 3 by the storage cells 101, 301, in combination with the transistors 112, 113 and the inverter 114 and by the storage cells 201, 401 in combination with the transistors 212, 213 and the inverter 214, which in each case commonly represent a trigger stage. As already described with reference to Fig. 2, the drive circuit ensures that the erasing voltage of each individual storage cell is disconnected when a cell which is to be erased has fallen below a specific given threshold voltage. Via the inverters 114, 214 the reuction in a voltage U_D at 131 and U_{Dn+1} at 231 increases the gate voltages connected to the transistors 112, 212. Since, due to the presence of the signal τ, the transistors 113, 213 are switched on for the entire erasing processes, when the transistor 112, 212 is switched on the voltages connected at 131, 231 are further reduced. Following the undershooting of a threshold value of U_{Dn} and U_{Dn+1}, the circuit automatically switches into a stable end state where U_{Dn}, U_{Dn+1} are close to 0 V. The switching process simultaneously switches on the transistors 121, 221 and consequently the erasing voltages connected to the recharging zones 117, 217 and 317, 417 are reduced to small values. Again in Fig. 3, not until the end of the erasing process, is resetting effected by the blocking of the transistors 113, 213 since τ = 0. In order to terminate the entire erasing time of the store, the drain voltage of each selected cell, e.g. the drain voltages U_{Dn} of the selected cell in the n-th bit, can be fed via the output 141 along the drain line 140 via an inverter (not shown) to an AND gate β (not shown). Similar remarks apply to the drain voltage U_{Dn+1} of the $n+1$-th storage bit in respect of the output 241 and the drain line 240. Since a cell becomes conductive when it reaches the erased state, and thus the drain voltage falls from a previously positive value to a value of approximately 0 V, every erased cell applies a "0" to an inverter arranged at the output 141, and thus applies a "1" to an input of an AND gate β which is connected to the inverter. When the slowest cell of a selected word has reached the erasing state, all the inputs of the AND gate β carry a "1" so that the output emits a "1". This end signal can be directly used to terminate the erasing time τ of the store.

A drive circuit as illustrated in Fig. 3 and one-transistor storage cells as provided in Fig. 3 can be used to erase a store pulse-wise

similarly to Fig. 2. As can be seen from the drawing, the drive circuit as represented in Fig. 3 allows a reduction in components in comparison to a drive circuit as illustrated in Fig. 2, and also facilitates more rapid read-out.

In the drive circuit as represented in Fig. 3 it is also possible to erase a store not pulse-wise but by means of an erasing voltage which is constant in terms of time with simultaneous check read-out. In this case, however, it must be borne in mind that the non-selected storage cells whose gate voltages correspond to a high compensation voltage during the erasure process, are highly conductive and therefore would disturb the check read-out process. Under these circumstances either an additional selector transistor, thus a two-transistor storage cell, is required (unless the store consists only of one single word).

Stores of the type described can be used for tuning stores or numerical stores, e.g. in telephone exchange equipment.

CLAIMS

1. A non-volatile semiconductor store which can be electrically erased word-wise, comprising a matrix of storage cells, control means operable to apply voltages to selected storage cells for erasure thereof, and monitoring means arranged, in use, to monitor, the state of the storage cells during erasure and to recognise when each cell being monitored reaches its erased state.

2. A store according to claim 1, in which the control means is arranged in operation to supply erasing voltages to the selected storage cells intermittently in the form of pulses, and the monitoring means is arranged to monitor the state of the storage cells during the intervals between the pulses.

3. A store according to claim 1, in which the control means is arranged in operation to supply erasing voltages to the selected storage cells continuously whereby erasure and monitoring take place simultaneously.

4. A store according to any one of claims 1 to 3, in which the monitoring means is arranged in operation to recognise erasure of the cells being monitored as being complete when they have a threshold voltage less than or equal to a predetermined value.

5. A store according to claim 4, in which the monitoring means is arranged to monitor the threshold voltage by monitoring the drain voltages of the cells whilst a voltage equal to said predetermined value is applied to the gates thereof.

6. A store according to any one of the preceding claims, in which the monitoring means is arranged upon said recognition to terminate the application of said voltages by the control means to the respective cell thereby terminating the erasure process.

7. A store according to any one of the preceding claims, in which the gate lines of the field effect transistors which are used to construct storage cells run from word to word and the associated drain lines run from bit to bit.

8. A store as claimed in any one of the preceding claims, including a potential divider arranged to supply the gate voltage which is required as predetermined threshold voltage value for check read-out during erasure, and a gate voltage for the read-out of the store so that the former is always smaller than the latter.

9. Stores substantially as herein described with reference to the accompanying drawings.

Printed for Her Majesty's Stationery Office
by Burgess & Son (Abingdon) Ltd.—1980.
Published at The Patent Office, 25 Southampton Buildings,
London, WC2A 1AY, from which copies may be obtained.